Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, said oxidizing step producing a plurality of bird's beak structures at the edges of said at least one dielectric trench where said nitride layer is discontinued, and a filling step of said at least one trench with a filling material; ~~and~~

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench; and

planarizing the surface of said semiconductor device by removing said plurality of bird's beak structures and etching back said filling material.

2. (Previously Presented) The integration process of claim 1 wherein said oxidizing step of said sidewalls of said at least one dielectric trench does not plug the at least one dielectric trench dielectrically, and that said nitride layer on the surface of said semiconductor device prevents oxide from being grown during said oxidizing step.

3. (Original) The integration process of claim 1, further comprising a step of removing said hardmask nitride layer, and a further step of growing an oxidation layer on the surface of said semiconductor device.

4. (Original) The integration process of claim 3, comprising a further step of removing said oxide layer.

5.-6. (Cancelled)

7. (Currently Amended) The integration process of claim ~~5~~ 1 wherein said oxidizing step places said walls of said trench in direct contact with at least one doped surface layer.

8. (Original) The integration process of claim 1 wherein a filling material is used, during said step of filling said at least one trench, said filling material having a sufficient thickness to plug up said at least one dielectric trench.

9. (Original) The integration process of claim 1, further comprising a step of doping said filling material.

10. (Original) The integration process of claim 9 wherein said doping step is carried out during a step of implanting at least one implanted layer needed to form components to be integrated in said well.

11. (Original) The integration process of claim 9 wherein said doping step is carried out *in situ* during said filling step.

12. (Original) The integration process of claim 9 wherein said doping step comprises a further oxidizing step of a pre-implantation oxide layer, and an enhancement implanting step carried out on the entire surface of said semiconductor device.

13. (Currently Amended) The integration process of claim ~~5~~1, further comprising a step of forming sinker layers in said well.

14. (Previously Presented) The integration process of claim 13 wherein said step of forming sinker layers comprises at least one masking step of said well, carried out using a masking resist layer to define openings at the locations of said sinker layers, followed by an implanting step.

15. (Original) The integration process of claim 14 wherein said masking resist layer is set back from said bird's beak structures.

16. (Original) The integration process of claim 14 wherein said masking resist layer is removed from around said at least one oxidized trench on said well side.

17. (Previously Presented) The integration process of claim 1, further comprising masking, implanting, and annealing steps directed to produce doped layers before forming the active areas.

18. (Previously Presented) The integration process of claim 1 wherein said active area forming step comprises at least one depositing step of an additional nitride layer, and a step of photomasking and etching said additional nitride layer at the locations of field regions.

19. (Original) The integration process of claim 18 wherein said further nitride layer is removed from said at least one trench to isolate said filling material.

20. (Original) The integration process of claim 18 wherein said additional nitride layer is not removed from said at least one trench, thereby establishing a contact to said filling material.

21. (Original) The integration process of claim 18, further comprising an oxidizing step effective to form a field oxide layer over said field regions and a second plurality of bird's beak structures at the edges of said field regions where said additional nitride layer is discontinued.

22. (Original) The integration process of claim 21 wherein said oxidizing step is preceded by a step of integrating a portion of doped layer effective to oppose formation, from said oxidizing step, of interspace surface junctions in the neighborhood of said field regions.

23. (Previously Presented) The integration process of claim 1 wherein said nitride layer is used for said active area forming step, and that it comprises at least one step of photomasking and etching said nitride layer away from sinker regions.

24. (Cancelled)

25. (Previously Presented) The integration process of claim 13 wherein said step of forming sinker layers comprises at least one step of masking said nitride layer in order to define openings at the locations of said sinker layers, followed by an implanting step.

26. (Original) The integration process of claim 25, further comprising a step of removing a thick oxide layer from said at least one dielectric trench.

27. (Original) The integration process of claim 1, comprising a further step of removing said nitride layer after said step of forming said at least one dielectric trench.

28. (Original) The integration process of claim 27, comprising a further step of removing said oxide layer after said further step of removing said nitride layer.

29. (Previously Presented) The integration process of claim 27 wherein said oxidizing step of said sidewalls of said at least one dielectric trench further comprises growing a further oxide layer over the surface of said semiconductor device.

30. (Original) The integration process of claim 27 wherein said active area defining step comprises a step of masking and etching said further oxide layer.

31. (Previously Presented) The integration process of claim 3, further comprising before said step of removing said hardmask nitride layer, an oxidizing step effective to form an oxide layer over the surface of said filling material of said at least one trench.

32. (Previously Presented) The integration process of claim 1 wherein the thickness of said nitride layer used as a hardmask is adequate to ensure performance during subsequent etching steps directed to form said at least one dielectric trench.

33. (Original) The integration process of claim 32 wherein a value of less than 3 or 4 is selected for the ratio between said nitride layer thickness used as a hardmask and an oxide layer thickness.

34. (Original) The integration process of claim 1, further comprising a step of coating the surface of said semiconductor device with a protective resist layer, and a step of backetching the back side of said semiconductor device.

35. (Previously Presented) The integration process of claim 34, further comprising a step of removing said nitride layer and said oxide layer, and an oxidizing step

effective to form, on the surface of said semiconductor device, a layer of pre-implantation oxide for said step of defining active areas of components to be integrated in said well.

36. (Original) The integration process of claim 1 wherein said at least one dielectric trench is formed to contact a buried oxide layer underlying said substrate and effective to provide vertical insulation for said well.

37. (Original) The integration process of claim 36, comprising a step of forming at least a second dielectric trench providing, jointly with said at least one dielectric trench and said buried oxide layer, a trench insulating structure for said well.

38.-40. (Cancelled)

41. (Currently Amended) ~~A~~ An integration process for ~~forming~~ semiconductor devices having a dielectrically insulated well in connection with an SOI substrate, comprising:

forming an oxide layer on the SOI substrate;

forming a nitride layer on the oxide layer;

forming a mask using a resist layer directly on the nitride layer to define photolithographic openings for forming at least one dielectric trench;

etching the nitride layer and the oxide layer through the photolithographic openings with the nitride layer used as a hard mask; and

forming at least one dielectric trench, comprising etching the SOI substrate to form the at least one dielectric trench with sidewalls; and oxidizing the sidewalls of the at least one dielectric trench;

filling the at least one dielectric trench with a filling material and doping the filling material, the step of doping carried out during a step of implanting at least one implanted layer needed to form components to be integrated in the well; and

coating the surface of the semiconductor device with a protective resist layer and back etching the back of the semiconductor device.

42. (Previously Presented) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, and a filling step of said at least one trench with a filling material and doping the filling material, the step of doping carried out during a step of implanting at least one implanted layer needed to form components to be integrated in the well; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench.

43. (Previously Presented) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, and a filling step of said at least one trench with a filling material; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench, the active area forming step further comprising at least one step of depositing an additional nitride layer and a step of photomasking and etching the additional nitride layer at locations of field regions and not removing the additional nitride layer from the at least one trench to establish a contact with the filling material.

44. (Previously Presented) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, and a filling step of said at least one trench with a filling material; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench, the acting area forming step comprising at least one step of depositing an additional nitride layer and a step of photomasking and etching the additional nitride layer at locations of field regions, and an oxidizing step effective to form a field oxide layer over the field regions and a second plurality of bird's beak structures at the edges of the field regions where the additional nitride layer is discontinued, the oxidizing step preceded by a step of integrating a portion of doped layer

effective to oppose formation, from the oxidizing step, of interspace surface junctions in the neighborhood of the field regions.

45. (New) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, and a filling step of said at least one trench with a filling material; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench, the nitride layer used for said active area forming step and comprising at least one step of photomasking and etching said nitride layer away from center regions.

46. (New) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, and a filling step of said at least one trench with a filling material;

forming sinker layers comprising at least one step of masking said nitride layer in order to define openings at the locations of said sinker layers, followed by an implanting step; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench.

47. (New) An integration process in a SOI substrate of a semiconductor device including at least a dielectrically insulated well, the process comprising:

an oxidizing step directed to form an oxide layer;

a depositing step of a nitride layer onto said oxide layer; and

a masking step, carried out onto said nitride layer using a resist layer and directed to define photolithographic openings for forming at least one dielectric trench effective to provide side insulation for said well;

an etching step of said nitride layer and said oxide layer, as masked by said resist layer, said nitride layer used as a hardmask;

a step of forming said at least one dielectric trench and comprising at least one etching step of said substrate, an oxidizing step of at least sidewalls of said at least one dielectric trench, removing a thick oxide layer from said at least one dielectric trench, and a filling step of said at least one trench with a filling material;

forming sinker layers comprising at least one step of masking said nitride layer in order to define openings at the locations of said sinker layers, followed by an implanting step; and

a step of forming active areas for components to be integrated in said well, being carried out after said step of forming said at least one dielectric trench.